UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,664	07/28/2004	Te-Chih Chang	AMIP0029USA	4663

27765 7590 10/04/2005

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
COX, CASSANDRA F	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,664	CHANG, TE-CHIH	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-11* is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Objections

2. Claim 1 is objected to because of the following informalities: In claim 1, each occurrence of the label "RCM" should be replaced by the word --reset--, to clarify that it is a reset signal that is being output. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 4-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Whiteside (U.S. Patent No. 5,142,555).

In reference to claim 1, Whiteside discloses in Figure 5a a digital phase frequency discriminator (which are also known as phase frequency detectors) comprising: a first SR latch (206, 208) for generating a first output signal (205) when

being set to a predetermined state, the first SR latch (206, 208) comprising a first input end for receiving a first input signal (201); a second SR latch (218, 216) for generating a second output signal (215) when being set to the predetermined state, the second SR latch (218, 216) comprising a first input end for receiving a second input signal (211); a predetermined state detection circuit (210) electrically connected to the first (206, 208) and the second (218, 216) SR latches for detecting the first and second output signals (205, 215) and for outputting a reset signal; a first predetermined state control circuit (202, 204) electrically connected to the predetermined state detection circuit (210) and the first SR latch (206, 208) for setting the first SR latch (206, 208) to the predetermined state according to the reset signal, the first predetermined state control circuit (202, 204) comprising a first input end for receiving the first input signal (201), and a second input end for receiving the reset signal; and a second predetermined state control circuit (214, 212) electrically connected to the predetermined state detection circuit (210) and the second SR latch (218, 216) for setting the SR latch (218, 216) to the predetermined state according to the reset signal, the second predetermined state control circuit (214, 212) comprising a first input end for receiving the second input signal (211), and a second input end for receiving the reset signal.

In reference to claim 4, Whiteside discloses in Figure 5a wherein the predetermined state detection circuit comprises a NAND gate (210).

In reference to claim 5, Whiteside discloses in Figure 5a wherein the first SR latch (206, 208) comprises a Q output signal end (Q_1), the second SR latch (218, 216)

comprises a Q output signal end (Q_2), and the NAND gate (210) comprises two input ends electrically connected to the two Q output signal ends respectively.

In reference to claim 6, Whiteside discloses an alternate embodiment in Figure 5b wherein the predetermined state detection circuit comprises a NOR gate which is well known to one skilled in the art to be the equivalent of an OR gate coupled with an inverter, of which fact official notice is taken.

In reference to claim 7, Whiteside discloses in Figure 5b wherein the first SR latch (the upper two cross-coupled NAND gates) comprises a Qbar output signal end ($Qbar_1$), the second SR latch (the lower two cross-coupled NAND gates) comprises a Qbar output signal end ($Qbar_2$), and the OR gate (which is the equivalent of the NOR gate laid out as an OR gate coupled with an inverter as mentioned above with respect to claim 6) comprises two input ends electrically connected to the two Qbar output signal ends respectively.

In reference to claim 8, Whiteside discloses in Figure 5a wherein both the first (206, 208) and the second (218, 216) SR latches comprise a pair of cross-coupled NOR gates.

In reference to claim 9, Whiteside discloses in Figure 5b wherein both the first and the second SR latches comprise a pair of cross-coupled NAND gates.

In reference to claim 10, Whiteside discloses in Figure 5a wherein both the first (202, 204) and the second (214, 212) predetermined state control circuits comprise a pair of cross-coupled NAND gates.

In reference to claim 11, Whiteside discloses in Figure 5b wherein both the first (the upper two cross-coupled NOR gates) and the second (the lower two cross-coupled NOR gates) predetermined state control circuits comprise a pair of cross-coupled NOR gates.

Allowable Subject Matter

5. Claims 2-3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Claims 2-3 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 11 wherein the circuit further comprises a first delay (300) connected between the first input end of the first predetermined state control circuit (56) and the first input end of the first SR latch (52) in combination with the rest of the limitations of the base claims and any intervening claims. Suzuki discloses a first delay (83) connected between the first input signal (REF) and both the first inputs of the first predetermined state control circuit (81) and the first SR latch (79).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-

1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC
CC
September 29, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800